

## Conducted emission study in space vector modulated voltage source inverter

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### ABSTRACT

To comply with electromagnetic interference (EMI) standards, the electromagnetic noise generated by power electronic converters must be analyzed and suppressed since the switching frequency of the converter affects EMI noise. Conducted emission occurs in drive systems due to inverter parasitic capacitances and rapidly switching inverter output voltages. The EMI noise produced space vector pulse width modulation (SVPWM) inverter is calculated using MATLAB/Simulink simulation data. The unwanted common mode and differential mode signals produced by the inverter are captured using a spectrum analyzer and examined using short time Fourier transform (STFT). To mitigate the effect of EMI in the circuit and to comply with the standards filters are developed. The passive filter components are defined by the EMI standards attenuation requirements. The MATLAB simulation findings are confirmed and verified by hardware implementation.

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## 1. INTRODUCTION

Operating characteristics of inverters has significantly improved due to the advent of high-speed switching of electronic devices. Conducted and radiated electromagnetic interferences are generated due to the fast-switching action. For practical applications adherence of the power electronic circuit to electromagnetic compatibility is mandatory. Analysis of electromagnetic interference (EMI) of power converters at the design stage is important to avoid costly errors at the later stages of deployment of the converter. Hence, modelling of the dynamic behavior of the switching device, and accounting for various parasitic components is an indispensable part of EMI studies. EMI is caused due to common mode and differential mode noises [1]. Common mode (CM) and differential mode (DM) noises are to be analyzed analytically and its effect needs to be mitigated using appropriate mitigation techniques before actual hardware prototyping.

Research areas are focusing on addressing the complications imposed by the fast switching devices on PWM drive applications. EMI filter design for single-phase grid-connected inverter with noise source impedance consideration is presented in [2]. Frequency domain model for an inverter is presented by Drozhzhin [3]. Modified nodal analysis using state space average model is analyzed [4]. Bondarenko [5] has designed a power inverter and analyzed the Electromagnetic compatibility. Analysis of conducted emissions in the powertrain of electric vehicles is presented by Spadacini *et al.* [6]. Model for conducted emission of SiC Power Modules for automotive traction is presented in [7]. Detailed study on conducted emissions of an

inverter for filter development in high voltage networks is researched [8]. Soft switching topologies also reduce the current distortion [9]. Soft switching for inverter and the effect on EMI mitigation is presented in [10]-[12]. Hard switching power losses are higher compared to soft switching due to fixed value of the DC VOLTAGE in hard switching and a sinusoidal oscillation of the DC voltage in soft switching. Hanioka *et al.* [13] has researched on switching control method for voltage-source PWM inverters to eliminate conduction noise between phases. Common-mode EMI comparison for different PWM techniques is explained in [14]. Noise reduction method for three-level V-connected inverter using SVPWM is analyzed by Itoh *et al.* [15].

In this paper a SVPWM based three phase inverter is analyzed in detail and the switching configurations are simulated in MATLAB. For conducted emission estimation the equivalent circuit of the inverter is analyzed in MATLAB. The harmonic currents are measured by inserting standard line impedance stabilization network (LISN) in the power line. The common mode and differential mode noises generated at the point of coupling between the LISN and converter under test is measured using spectrum analyzer. The measurement values obtained in the spectrum analyzer depicts the noise levels generated by the converter. To comply with the stipulated EMI EMC regulatory standards 3rd order EMI power line filter is designed to attenuate the noise levels beyond 150 kHz and maintain the noise levels within the specified band. The prototype of the SVPWM based 3 phase inverter and EMI filter was realized in hardware and tested for conducted emission.

## 2. SVPWM BASED MODULATION SCHEME

SVPWM is a technique used to calculate the PWM signals for the switches to generate the required 3-phase voltages for the motor. It is widely used in industrial application due to efficient use of DC bus voltage, reduction in harmonic distortion, and relatively easier digital implementation [16]. Space-vector is a single complex number representing the combined effect of all three phase currents in an AC machine at a particular instant of time. Vector sum is obtained by adding the three vectors and its magnitude is always constant. The operation of the three phase inverter is governed by six switches shown in Figure 1, comprising of eight inverter configurations.

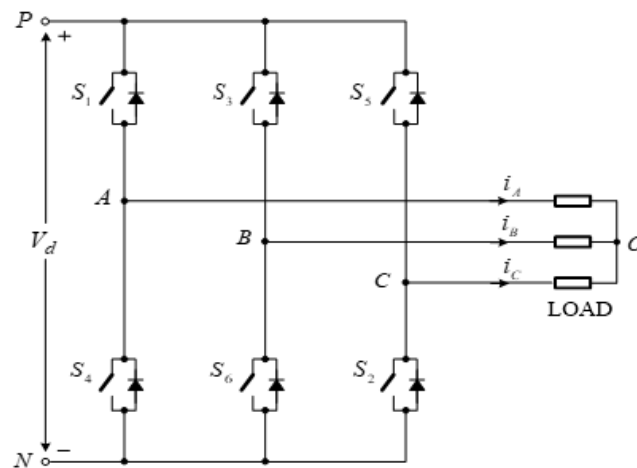


Figure 1. Three phase inverter configuration

Each configuration is mapped into corresponding space vectors. In each configuration, '0' represents negative phase voltage level and a '1' represents positive phase voltage level. Necessary pulses are generated to sequentially turn the inverter switches (IGBTs) ON and OFF. To prevent vertical conduction appropriate care needs to be taken to prevent overlapping during transition of switches. Two adjacent voltage vectors are selected based on the sector in which the reference vector is present. The voltage vectors are represented in a binary format and differ only by one bit, so that the transition from one adjacent vector to the other requires the operation of only one switch at a time. The two vectors are weighted according to time, during a sampling period of time T to give the required output voltage as shown in Table 1. The reference vector selects two neighboring voltage vectors. The voltage vectors are stored in binary and vary only by one bit, thus switching between them needs just one switch at a time.

Table 1. Switching configuration

	Switch ON	Vector
[111]	S <sub>1</sub> ,S <sub>3</sub> ,S <sub>5</sub>	$\vec{V}_0 = 0$
[000]	S <sub>4</sub> ,S <sub>6</sub> ,S <sub>2</sub>	
[100]	S <sub>1</sub> ,S <sub>6</sub> ,S <sub>2</sub>	$\vec{V}_1 = \frac{2}{3}V_d e^{j0}$
[110]	S <sub>1</sub> ,S <sub>3</sub> ,S <sub>2</sub>	$\vec{V}_2 = \frac{2}{3}V_d e^{j\frac{\pi}{3}}$
[010]	S <sub>4</sub> ,S <sub>3</sub> ,S <sub>2</sub>	$\vec{V}_3 = \frac{2}{3}V_d e^{j\frac{2\pi}{3}}$
[011]	S <sub>4</sub> ,S <sub>3</sub> ,S <sub>5</sub>	$\vec{V}_4 = \frac{2}{3}V_d e^{j\frac{3\pi}{3}}$
[001]	S <sub>4</sub> ,S <sub>6</sub> ,S <sub>5</sub>	$\vec{V}_5 = \frac{2}{3}V_d e^{j\frac{4\pi}{3}}$
[101]	S <sub>1</sub> ,S <sub>6</sub> ,S <sub>5</sub>	$\vec{V}_6 = \frac{2}{3}V_d e^{j\frac{5\pi}{3}}$

Assume the voltage reference vector,  $V_{ref}$ , lies in the first sector as shown in Figure 2, between the standard vectors  $V_1$  and  $V_2$ .  $V_{ref}$  is produced by a combination of  $V_1$  and  $V_2$ . If the duration of the pulse is  $T$ , the period for which for vectors  $V_1$  and  $V_2$  will be ON are:

$$T_r = \frac{|V_1|}{|V_{ref}|_{max}} * T, T_l = \frac{|V_2|}{|V_{ref}|_{max}} * T \quad (1)$$

Where  $|V_{ref}|_{max}$  is equal to two-thirds of the applied DC voltage to the inverter.  $|V_{ref}|_{max}$  and  $T$  are known quantities. The values of  $V_1$  and  $V_2$  can be determined from Table 2.

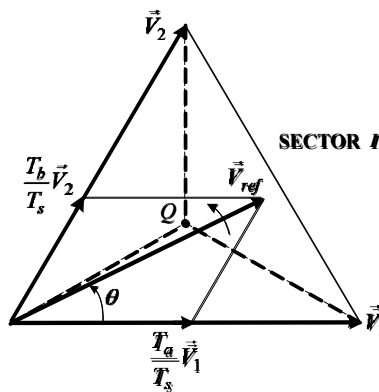


Figure 2. Space vector representation-sector I

Table 2. Calculation of  $u_r$ ,  $u_l$  and time for various sectors and quadrants

State	Quadrant	$ V_l $ (approximation for $V_1$ )	$ V_l $ (approximation for $V_2$ )	Switching time
1	Q1	$ u_{s\alpha}  - \frac{1}{\sqrt{3}} u_{s\beta} $	$\frac{2}{\sqrt{3}} u_{s\beta} $	$T_a = T_r + T_l + (T_0/2); T_b = T_l + (T_0/2); T_c = (T_0/2);$
2	Q1	$ u_{s\alpha}  + \frac{1}{\sqrt{3}} u_{s\beta} $	$- u_{s\alpha}  + \frac{1}{\sqrt{3}} u_{s\beta} $	$T_a = T_l + (T_0/2); T_b = T_r + T_l + (T_0/2); T_c = (T_0/2);$
	Q2	$- u_{s\alpha}  + \frac{1}{\sqrt{3}} u_{s\beta} $	$ u_{s\alpha}  + \frac{1}{\sqrt{3}} u_{s\beta} $	
3	Q2	$\frac{2}{\sqrt{3}} u_{s\beta} $	$ u_{s\alpha}  - \frac{1}{\sqrt{3}} u_{s\beta} $	$T_a = (T_0/2); T_b = T_r + T_l + (T_0/2); T_c = T_l + (T_0/2);$
4	Q3	$ u_{s\alpha}  - \frac{1}{\sqrt{3}} u_{s\beta} $	$\frac{2}{\sqrt{3}} u_{s\beta} $	$T_a = (T_0/2); T_b = T_l + (T_0/2); T_c = T_r + T_l + (T_0/2);$
5	Q3	$ u_{s\alpha}  + \frac{1}{\sqrt{3}} u_{s\beta} $	$- u_{s\alpha}  + \frac{1}{\sqrt{3}} u_{s\beta} $	$T_a = T_l + (T_0/2); T_b = (T_0/2); T_c = T_r + T_l + (T_0/2);$
	Q4	$- u_{s\alpha}  + \frac{1}{\sqrt{3}} u_{s\beta} $	$ u_{s\alpha}  + \frac{1}{\sqrt{3}} u_{s\beta} $	
6	Q4	$\frac{2}{\sqrt{3}} u_{s\beta} $	$ u_{s\alpha}  - \frac{1}{\sqrt{3}} u_{s\beta} $	$T_a = T_r + T_l + (T_0/2); T_b = (T_0/2); T_c = T_l + (T_0/2);$

During the pulse period  $T$ , the vectors  $V_1$  and  $V_2$  are applied for duration of  $T_r$  and  $T_l$  respectively. In the remaining time period, i.e.,  $T - (T_r + T_l)$ , either of the two zero vectors  $V_0$  or  $V_7$  are applied. If the previous switching state was  $V_0$ , and then the sequence would be  $V_0, V_1, V_2$  and  $V_7$ . If the last switching state was  $V_7$ , then the sequence is  $V_7, V_2, V_1$  and  $V_0$ . SVPWM for a three phase inverter was simulated in MATLAB. The parameters used for simulation are tabulated in Table 3.

First three phase to two phase transformation (Clarke transformation) is performed, the corresponding sector is identified and then the switching vector for each sector is calculated. Using volt second balance the active vector timing is estimated and then the gating time period for each leg is calculated. The three phase voltage waveform generated using SVPWM technique for modulation index of 0.5 is shown in Figure 3.

Table 3. Design specification

Parameter	Value
Max. DC bus voltage	48 VMax
Output power	200 WMax
Switching frequency	25 kHz

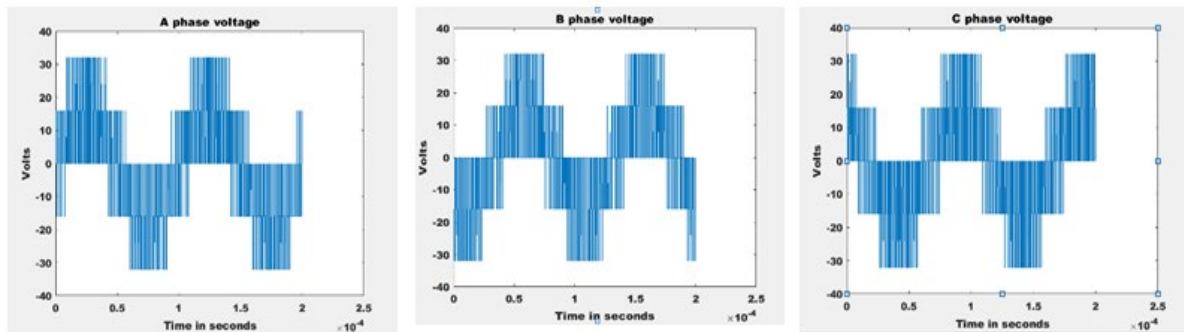


Figure 3. Three phase voltage wave form generated using SVPWM

### 3. CONDUCTED EMISSION FOR 3 PHASE INVERTER

Rapid turn on and turn off of power transistor causes abrupt disruptions in current flow, leading to high voltage ringing and spikes. Study of EMI and filter design is dictated by the deployment condition, EMI standard, noise source and propagation path conditions. EMI analysis and filter design can be challenging, necessitating a time-consuming iterative process of design, testing, and redesign. Conducted EMI noise analysis and filter design can be predicted to speed up the process of meeting EMI requirements. The objective of modeling is to analyze the noise emissions at the preliminary design stage.

#### 3.1. Noise: Common mode and differential mode

The phase currents can be characterized by differential and common mode (DM&CM) analysis [17]. The peak CM voltage occurs at zero vectors, whose duration is modulation index dependent. Harmonics are generated due to the distorted currents. Since, the amplitudes and harmonic components change with time, conventional Fourier transform, is not sufficient. Study based on short time Fourier transform (STFT) is used to determine the frequency and phase of local segments of a signal as it changes over time [18]. STFT computes the Fourier transform on each shorter segment of a larger temporal signal.

#### 3.2. Simulation of conducted emission of the converter

For simulating the common-mode noise, capacitive coupling ( $C_b$ ) between the circuit and ground plane and also capacitance between the ground plane and switching node ( $C_s$ ) is included. Ideal line impedance stabilization networks (LISNs) are placed between each terminal of the DC supply and the inverter to provide a standard impedance and measurement port for the noise [18]. The CM excitation is captured in a spectrum analyzer as shown in Figure 4.

Conducted emissions tests for automotive electronics should comply with CISPR 25 or EN 55025 standards. A per guidelines of CISPR 25 [19], noise signal at LISN is to be measured to study the EMC behavior. Voltage across the 50-ohm resistor is shown in Figure 5(a) and Figure 5(b). It can be seen that the

harmonics depends on the switching frequency. Common mode voltage ( $V_{cm}$ ) and differential mode voltage ( $V_{dm}$ ) can be calculated as [20]. Implementation of (2) and (3) is shown in Figure 6.

$$V_1 = V_{cm} + V_{dm}, \quad V_2 = V_{cm} - V_{dm} \quad (2)$$

$$V_{cm} = \frac{V_1 + V_2}{2}, \quad V_{dm} = \frac{V_1 - V_2}{2} \quad (3)$$

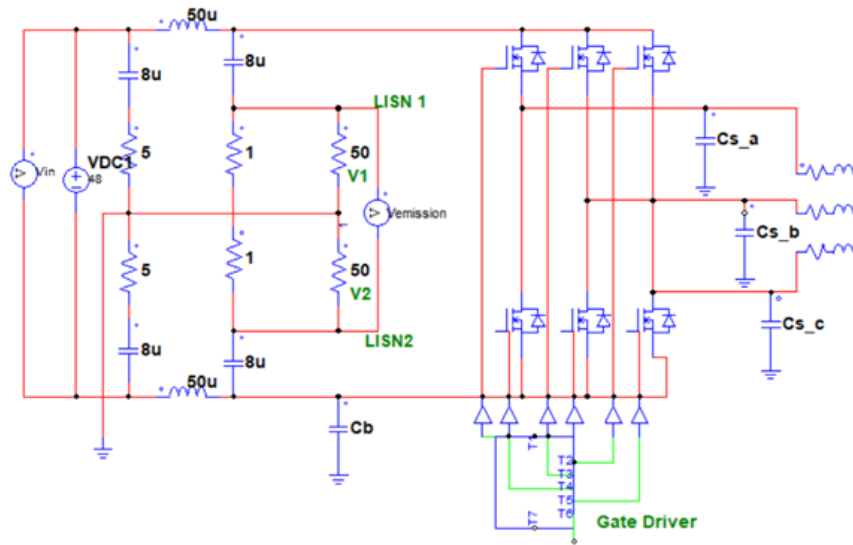


Figure 4. Simulation of conducted emission of the converter with LISN inserted at the input

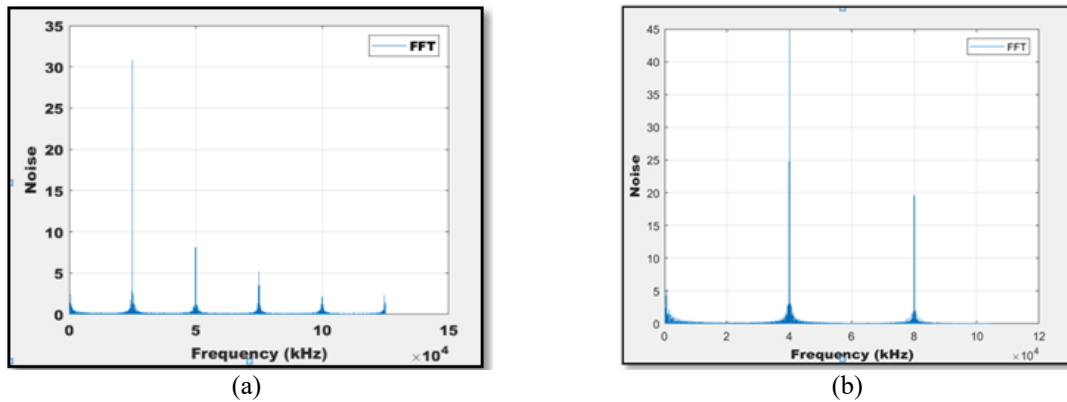


Figure 5. Fast Fourier transform (FFT) analysis of the noise signal at switching frequency (a) 25 kHz and (b) 40 kHz

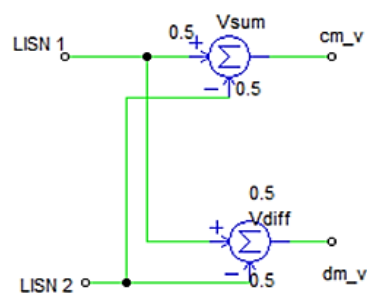


Figure 6. Separation of CM and DM from LISN output

The sample frequency is 500 kHz ( $\gg 2 \times 150$  kHz) and STFT is applied to the collected signal. The average of the FFT results for each 200 ms window is calculated. Figure 7(a) and Figure 7(b) indicate that the interference voltage values between 150 kHz and 100 MHz are above the CISPR 25 emission requirements mentioned in Table 4. Increasing the switching frequency from 25 kHz to 40 kHz also increases the noise levels.

Table 4. CISPR 25 Class5 EMI limit

Frequency of emission (MHz)	Conducted limit (dB $\mu$ V)	
	Quasi-peak	Average
0.15 - 0.3	57	50
0.53- 1.8	41	34
5.9-6.2	53	33
26-54	44	24
68-87	38	18
76-108	38	18

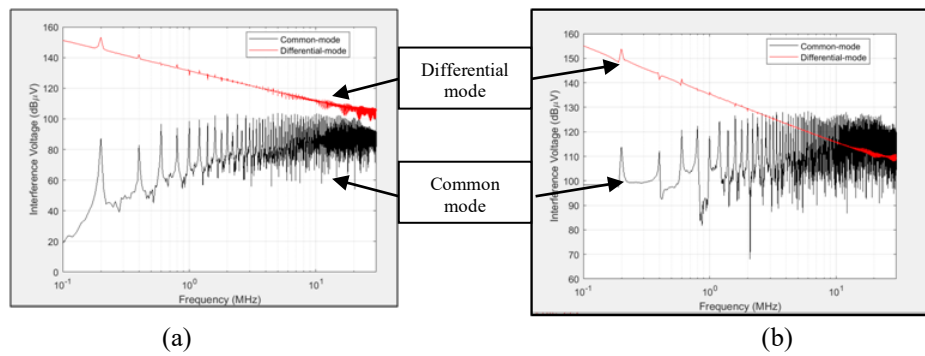


Figure 7. CM and DM noise for switching frequency (a) 25 kHz and (b) 40 kHz

#### 4. EMI FILTER DESIGN

EMI filters are designed to provide attenuation. The required corner frequency ( $f_c$ ) is determined based on the required attenuation ( $A$ ) of the noise at a particular frequency ( $f$ ) [21]-[23]. The attenuation for a third order filter and the required corner frequency ( $f_c$ ) to achieve the desired attenuation ( $A$ ) is given by (4). The chosen 3<sup>rd</sup> order filter topology is shown in Figure 8.

$$A[\text{dB}\mu\text{V}] = 60 \log \frac{f}{f_c}, f_c = f * 10^{\frac{-A}{60}} \quad (4)$$

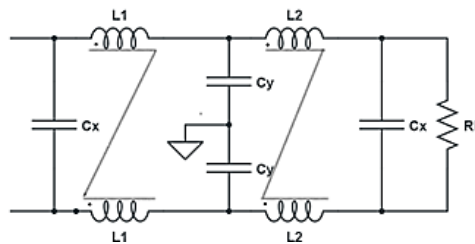


Figure 8. EMI filter

Common mode current is suppressed by inductors series with the power line and Y capacitors between the power line and ground. X capacitors between the lines minimize differential mode noise. Three poles (with the appropriate corner frequency) are added by inserting inductor between the second order low pass filter and the third pole (with the required corner frequency) [24], [25]. Figure 7 shows a noise level of 85 dB at 150 kHz, which is 25 dB higher than the intended use. For a 3<sup>rd</sup> order filter,  $f_c = 30$  kHz, and Load Resistance = 50. The inductance is calculated as:

$$L = \frac{R}{2\pi f_c} \quad (5)$$

$$\omega = 2\pi f_c = 18840 \text{ rad/sec} \quad (6)$$

Choosing damping factor,  $\zeta$  as 0.707 provides 3 dB attenuation at  $f_c$  and also controls filter ringing

$$\zeta = \frac{L\omega}{2R_L} = 0.707 \quad (7)$$

Choke,  $L_1 = 375 \mu\text{H}$  ( $L_1 = 1.1 \text{ mH}$ , to compensate for reduction or capacitance it is chosen 300% larger)

$$C_y = \frac{1}{L\omega^2} = 7.5 \mu\text{F} \quad (8)$$

#### 4.1. Design of third pole

$$\text{Choke, } L_2 = \frac{R_L}{2\pi f_c} = \frac{50}{2\pi \times 30000} = 0.2 \text{ mH} \quad (9)$$

$$f_n = \frac{R}{2\pi L_1} = 30030 \text{ Hz} \quad (10)$$

Attenuation at 150 kHz is 24 dB (second order filter) + 2.9 octave  $\times 6 = 41.4 \text{ dB}$ . X Capacitor: in differential mode, cut-off frequency of the filter is equal to  $f_{DM} = 150 \text{ kHz}$ .

$$C_x = \frac{1}{L_2 \omega^2} = 1.4 \mu\text{F} \quad (11)$$

FFT analysis of the signal captured across the LISN is shown in Figure 9. It can be seen that there is a considerable reduction in noise after insertion of the EMI filter as in Figure 10.

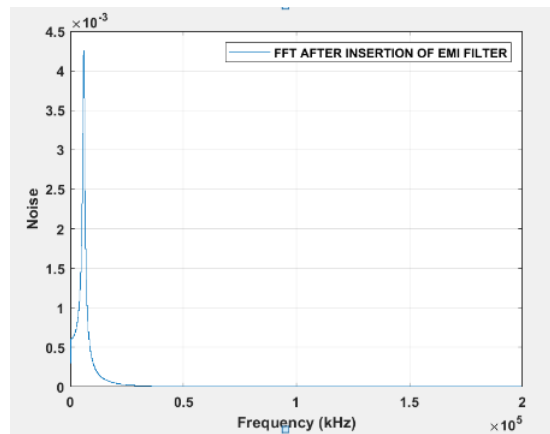


Figure 9. FFT analysis after insertion of filter

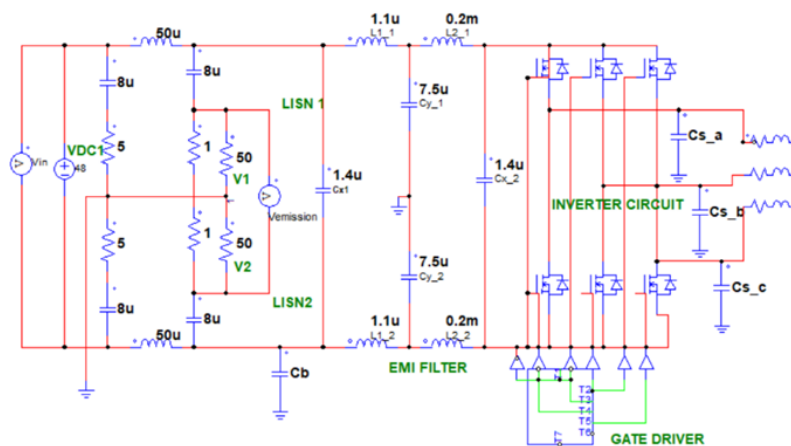


Figure 10. Simulation circuit with EMI filter

## 5. TEST SETUP AND RESULTS

The inverter model is validated by experimental investigation on the 200 W full-bridge inverter prototype designed using power MOSFET IRFP250 power module with a switching frequency of 25 kHz. A DC LISN is used to provide the defined impedance for the device. A test bench is used to perform the test and subsystems are placed as shown in the schematic diagram in Figure 11. A LISN's RF port connects directly to a spectrum analyzer. Initially, the projected emission level was at 85dBV, which is over the safety limits. Installation of the planned EMI filter between the power line and EUT, lowered emission rates to less than 40 dBV as in Figure 12 which is below the CISPR25 limits. The filter shields equipment from noise generated by DC power supply and other transient loads as well as noise generated by power converters. Because the peak and average values are less than those in Table 4, the power converter circuit meets the criteria.

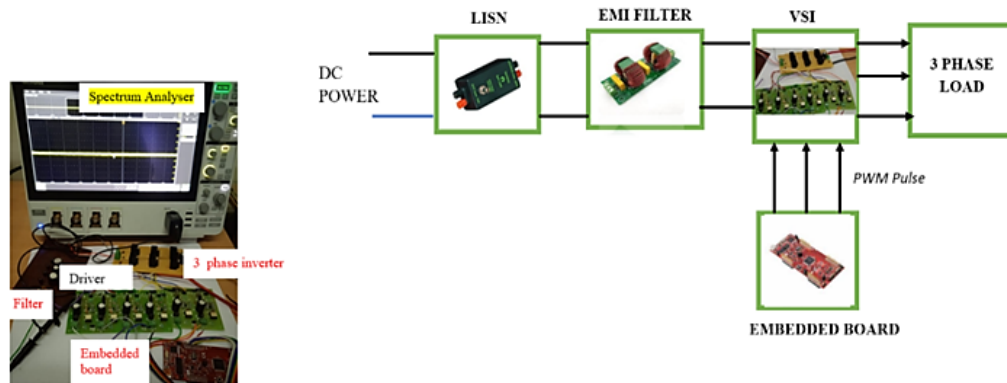


Figure 11. Test setup for inverter

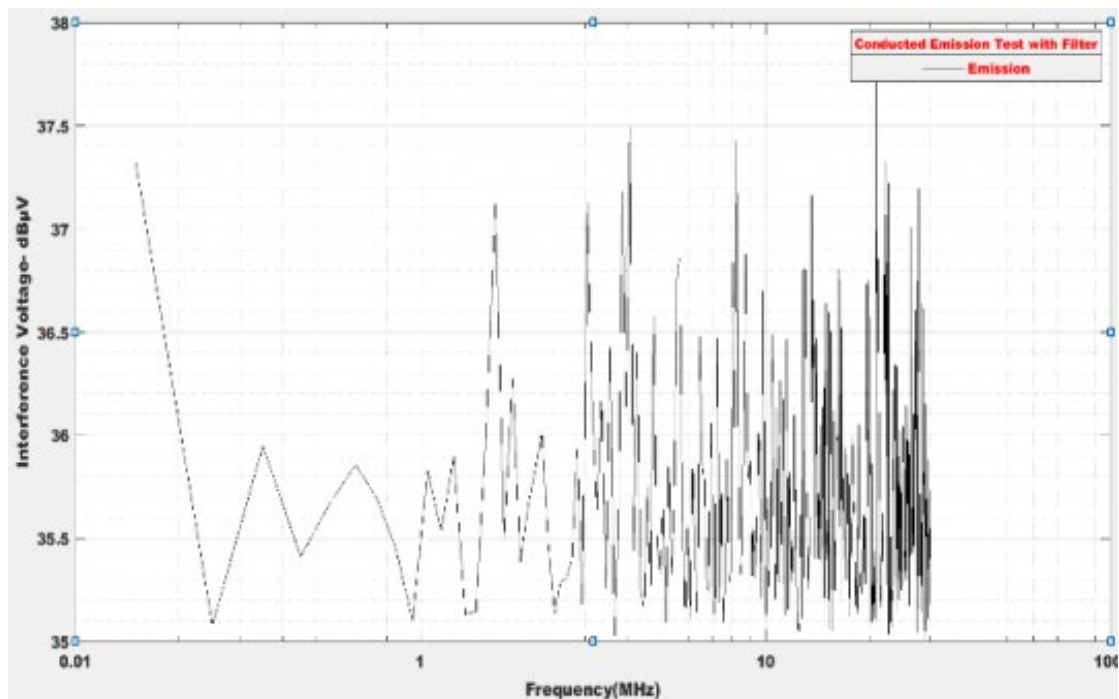


Figure 12. Noise after addition of EMI filter

## 6. CONCLUSION

In this work, SVPWM modulated three phase inverter is modelled and simulated to measure conducted emission. The emission levels are higher than expected standard level. EMI filter is designed to mitigate the common mode and differential mode noises. The common mode filter components are



constructed based on the insertion loss and required attenuations. The filter is placed in between the power supply and the inverter and conducted emission tests were performed. The noise levels are reduced, and it meets the CISPR 25 standards. The hardware prototype is also setup and measured. Power converters must have an EMI-compliant common mode filter to guarantee electromagnetic compatibility. Future study will examine the effect of the connecting cables and the three-phase load.




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